Hysteresis characteristics of hetero-structured devices using two-dimensional materials for memory applications

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Abstract

Recently, various hetero-structured devices using two-dimensional materials have been developed due to its high performances and flexibility.[1]-[3] In this work, the ultrathin memory devices consisting of two-dimensional (2D) materials were fabricated by stacking graphene, hexagonal boron nitride (hBN), and molybdenum disulfide (MoS_2), demonstrating large memory window and good retention properties as shown in Figure 1. The two different device structures of, graphene/hBN/MoS_2 (GBM) and MoS_2/hBN/graphene (MBG), where graphene and MoS_2 were employed as channel and charge trap layer for GBM and vice versa for MBG, were investigated. Even though both device structures exhibit a large hysteresis, their field effect transistor (FET) characteristics are quite different. The large hysteresis for memory application can be induced by quantum tunneling effect through the thin hBN layer (< 10 nm) and charge trapping in underlying 2D layer.[1],[4] By formation of the potential wells in the underlying MoS_2 or graphene layers between SiO_2 and hBN dielectrics, the charges can tunnel through ultrathin hBN layer and be effectively trapped or released depending on the applied gate voltages. We observed that these trapped charge can be maintained in potential wells and this induces the significant hysteresis in the current - voltage transfer curves of the 2D FETs. These results provide a promising way to fabricate memory devices using 2D materials.

References

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Figures

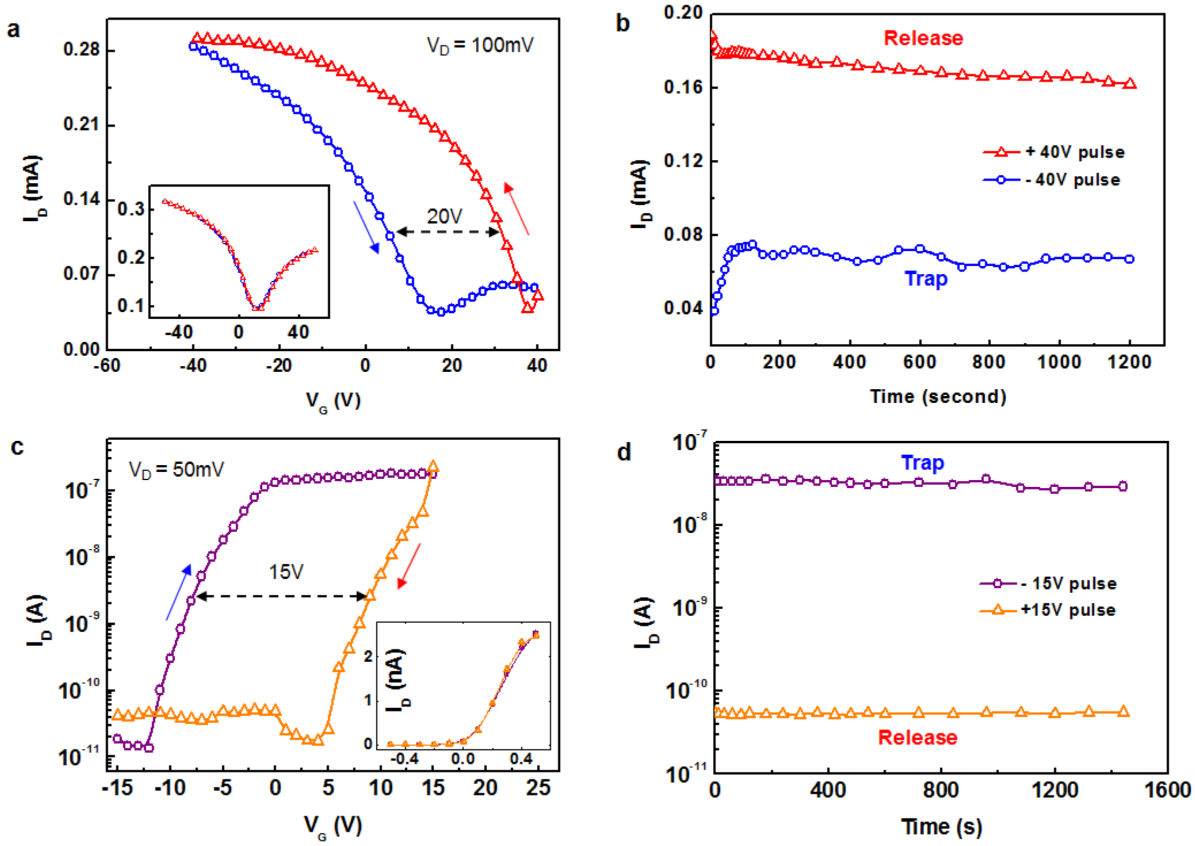

Figure 1. *(a) Transfer curve (I_D-V_G) and (b) Retention performance of the GBM device with hBN of 6 nm and MoS$_2$ of 5 nm. The inset of (a) shows a transfer curve of GB (Graphene/hBN). (c) Transfer curve and (d) Retention performance of the MBG device with hBN of 12 nm, MoS$_2$ of 3 layers, and graphene of 2 layers. The inset of (c) shows a transfer curve of the same device when graphene was used for gating.*